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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of
Bojkov et al.

Docket Number: **TI-35951**

Serial No.: **10/689,386**

Art Unit: **2811**

Filed: **October 20, 2003**

Examiner: **N. Parekh**

For: **DIRECR BUMPING ON INTEGRATED CIRCUIT CONTACTS ENABLED BY METAL-TO-INSULATOR ADHESION**

CERTIFICATION OF FACSIMILE TRANSMISSION

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NAME OF INVENTOR(S):
Bojkov et al.

TITLE OF INVENTION:
Direct Bumping on Integrated Circuit...

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT APPLICATION

Appl. No.	:	10/689,386	Confirmation No. 4156
Applicant	:	Christo P. Bojkov et al.	
Filed	:	October 20, 2003	
TC/A.U.	:	2811	
Examiner	:	Parekh, Nitin	
Docket No.	:	TI-35951	
Customer No.	:	23494	

BRIEF ON APPEAL

M. S. Appeal Brief-Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

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Jackie McBride

Jackie McBride

Dear Sir:

In support of their appeal of the Final Rejection of claims in this application, applicants respectfully submit this brief.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

This is an appeal of claims 1-22, all of the rejected claims. Claims 23-28 were canceled from the current examination. No claim is allowed.

STATUS OF AMENDEMNTS

Appellant did not file an amendment in response to the final rejection of April 28, 2005.

SUMMARY OF INVENTION

The invention directs to the structure of a semiconductor integrated-circuit device near a contact pad and the method of making the structure. The claimed subject matter involves the specific structure of a stack of protective layers over a portion of the contact pad and a metallic structure near the protective layers.

Claim 1

Claim 1 describes a contact pad structure (300) of a semiconductor integrated circuit chip device. The structure comprises two portions: the first portion is an ordered stack of protection layers over the surface of the chip and the second portion is an ordered stack of metal layer over the protection layer. The protection layers starts with a first inorganic layer (303) on the chip surface,[1] followed by a polymer layer (306) on the first inorganic layer (303),[2] and a second inorganic layer (310) on the polymer layer (303).[3] The metal layers starts with metallization (301) of the IC,[4] followed by a patterned seed metal layer (307) on the metallization (301) in the window[5] and on the second inorganic layer (310) around the window,[6] a buffer metal layer (308) positioned on the seed metal layer (307).[7]

Claims 2-19

Claims 2-19 properly depend from claim 1 with additional limitation. In particular, claim 2 further limits the metallization layer (301) in claim 1 to including copper;[8] claim 3 further limits the first inorganic layer (303) in claim 1 to including silicon nitride;[9] claim 4 further limits the first inorganic layer (303) in claim 1 to either silicon nitride, silicon oxynitride, silicon carbide, polyimide, or a stacked layer of these materials;[10] claim 5 further limits the first inorganic layer (303) in claim 1 to a thickness of about 0.5 to 2 μm;[11] claim 6 further limits the polymer layer (306) in claim 1 to including either benzocyclobutene or polybenzoxazole;[12] claim 7 further limits the polymer layer (306) in claim 1 to either polyimides, polyamic acids, polybenzoxazoles, benzocyclobutenes, polybenzocyclobutenes,

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[1] This application, p. 4, ll. 10-11.
[2] Ibid., p. 4, ll.11-12.
[3] Ibid., p. 4, ll.12-13.
[4] Ibid., p. 4, ll.13-14.
[5] Ibid., p. 4, ll.14-15.
[6] Ibid., p. 4, l.16.
[7] Ibid., p. 4, ll.16-18.
[8] Ibid., p. 4, ll.14-15.
[9] Ibid., p. 5, ll.1-3.
[10] Ibid., p. 5, ll.1-4.
[11] Ibid., p. 11, ll.8-10.
[12] Ibid., p. 11, ll.13-17.

or polysiloxanes;[13] claim 8 further limits the polymer layer (306) in claim 1 to a thickness of about 3 to 10 μm;[14] claim 9 further limits the second inorganic layer (310) in claim 1 to include silicon dioxide;[15] claim 10 further limits the second inorganic layer (310) in claim 1 to a dielectric of silicon dioxide, silicon nitride, silicon oxynitride, or a stacked layers thereof;[16] claim 11 further limits the second inorganic layer (310) to a thickness of about 0.5 to 2[17] μm; claim 12 further limits the seed metal (307) to include copper;[18] claim 13 further limits the seed metal (307) to overlap the second inorganic layer (307a) by about 5 to 15 μm;[19] claim 14 further limits the buffer metal (308) to a single metal layer;[20] claim 15 further limits the single metal layer (308) in claim 14 to include copper and copper alloy;[21] clam 16 further limits the buffer metal (308) in claim 1 to include a stack of metal layers;[22] claim 17 further limits the metal stack (308) in claim 16 to include a copper layer contacting the seed layer, a nickel layer on top of the copper layer, and a palladium layer as the outermost metal;[23] claim 18 further limits the structure in claim 1 to include a metal reflow element (309) attached to the buffer metal;[24] and claim 20 further limits the structure in claim 1 to include a bond wire (509) attached to the buffer metal.[25]

Claim 20

Claim 20 describes a structure of contact pad and a circuit metallization near the contact pad. It has all the limitations described in claim 1, with the addition limitation that the seed metal layer is patterned to form an extended trace (507) remote from the window.[26]

Claims 21 and 22

Claims 21 and 22 properly depend from claim 20 with additional limitations. In particular, claim 21 further limits the structure in claim 20 to include a metal reflow element

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[13] Ibid.
[14] Ibid., p. 11, ll.13-15.
[15] Ibid., p. 11, ll.22-24.
[16] Ibid., p. 11, ll.22-25.
[17] Ibid., p. 11, ll.8-10.
[18] Ibid., p. 12, ll.13-15.
[19] Ibid., p. 12, ll.21-23.
[20] Ibid., p. 12, l.31-p.13, l.1.
[21] Ibid., p. 12, l.31-p.13, l.3.
[22] Ibid., p. 13, ll.3-4.
[23] Ibid., p. 13, ll.4-7.
[24] Ibid., p. 13, ll.10-13.
[25] Ibid., p. 16, ll.1-5.
[26] Ibid., p. 14, ll.10-14.

(409) attached to the buffer metal;[27] and claim 22 further limits the structure in claim 20 to include a bond wire (509) attached to the buffer metal.[28]

ISSUES

Issue 1. Whether claim 1 is properly rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Wang et al. (US Pat. 6,782,897).

Issue 2. Whether claim 20 is properly rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Wang et al. (US Pat. 6,782,897).

GROUPING OF CLAIMS

The claims 1-19 stand or fall as a group; claims 20-22 stand or fall as a group. Although claims 1 and 20 stand rejected in the Final Office action for the exact same reason, they describe different inventions. Claim 20 has additional limitations over claim 1 that are not disclosed in the references and are not addressed in the Final Office action.

ARGUMENTS

Issue 1. Claim 1 is improperly rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Wang et al. (US Pat. 6,782,897) because the references relied in the Office Action do not support a case of prima facie obviousness against claim 1.

Applicant respectfully submits that the order of the stacked protection layers describes in claim 1 is not disclosed in the prior art references relied upon in the Office action. Claim 1 reads in part: said stack comprising a first inorganic layer on said surface (of an integrated circuit chip), a polymer layer on said first inorganic layer, and a second inorganic layer on said polymer layer. In other words, as shown in Figure 3, 4, and 5 of the application, the structure disclosed in claim 1 starts at the surface of the chip, on the surface of the chip is a first inorganic layer (303 in Fig. 3, 403 in Fig. 4, and 503 in Fig. 5), on the top of the first inorganic layer is a polymer layer (306 in Fig. 3, 406 in Fig. 4, and 506 in Fig. 5), and on top of the polymer layer is the second inorganic layer (310 in Fig. 3, 410 in Fig. 4, and 510 in Fig. 5) The cited references do not disclose this order.

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[27] Ibid., p. 14, ll.18-20.

The Office action argues that the claimed structure is achieved because the APA discloses a stack of a polymer layer on an inorganic layer and the Wang patent teaches a stack of passivation layer where the stack comprises a plurality of layers including a polymer layer and one or more layers of an inorganic material. This argument must fail for two reasons: First, the combination of the two prior references does not disclose the stack in claim 1; and second, there is no teaching, suggest, or motivation in the references to support combining layers in claim 1.

First, as conceded in the Office action, APA only discloses a stack of a polymer layer on an inorganic layer. APA does not disclose the second inorganic layer on the polymer layer; and the Wang patent does not disclose a second inorganic layer on the polymer layer either. This reason was presented to the Examiner in a response to an early Office action, which the Examiner deemed no persuasive. However, in rebutting this reasoning, the Final Office action only provided the two citations from the Wang patent.

The first citation directs to Col. 4, lines 49-53. This passage is copied below in its entirety:

> After the chip bonding pad 30 is formed, a passivation layer system 32, for example, including one or more layers of silicon nitride (SiN), polyimide, and Benzocyclobutene (BCD), are formed over the substrate surface 31 excluding an area overlying the chip bonding pad 30.[29]

There is no support that the passivation layer system has a second inorganic layer on a polymer layer. Therefore, even combining the APA and the Wang patent, there is still support that the stack in claim 1 is disclosed as claimed.

The second citation directs to the entire Brief-Description-of-the-Drawings Section and the entire Detailed-Description-of-the-Preferred-Embodiments Section of the Wang patent (col. 4-6). Yet, other than the passage copied above there is nothing in column 4 through column 6 of the Wang patent that lends addition support to a prima facie obviousness case against claim 1.

Because the prior art references do not disclose all the elements in claim 1, they do not render claim 1 obvious.

The Office Action further argues that the system in the Wang patent provides improved passivation and adhesion/bonding of the UBM layers. This argument must also fail because

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[28] Ibid., p. 16, ll.1-5.
[29] US 6,782,897 col. 4, ll. 48-53.

the Wang patent does not disclose the specific order of the layers and it is well established that "obvious to try" a modification or combination is not prima facie obviousness without a reasonable expectation of success.[30]

Second, there is no evidence in APA or the Wang patent to support a teaching, suggestion, or motivation that to incorporate the stack of protection layers including a second inorganic layer on the polymer layer, as argued in the Final Office action, so that the passivation and the adhesion/bonding can be improved, and delamination and stress can be reduced in the APA's device.[31]

In summary, applicants respectfully submit that the obviousness rejection against claim 1 is improper because the references do not disclose all the elements in claim 1 in the described order; there is no teaching, suggestion, or motivation for combining the elements in the order described in claim 1, and prima facie obviousness can not be established based on "obvious to try" a combination without a reasonable expectation of success. Because the Office action fails to establish a case of prima facie obviousness against claim 1, the 103 rejection is improper and claim 1 stands patentable over the references.

Issue 2. Claim 20 is improperly rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Wang et al. (US Pat. 6,782,897) because the references relied in the Office action do not support a case of prima facie obviousness against claim 20.

Claim 20 has a stacked protection layers, same as in claim 1. Claim 20 also has at one additional element of limitation: the seed metal layer being patterned to form an extended trace (507) remote from the window. The Office action rejects claim 20 for the exact reason it cites against claim 1; the fact that the additional element is not disclosed in the references was not address in the Final Office Action.

Therefore, applicants respectfully submit that for the same reason as presented regarding claim 1, the 103 rejection against claim 20 is also improper: the references do not disclose all the elements in claim 20 in the described order; there is no teaching, suggestion, or motivation for combining the elements in the order described in claim 20, and prima facie obviousness can not be established based on "obvious to try" a combination without a reasonable expectation of success. Because the Office action fails to establish a case of prima

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[30] See In re Geiger, 815 F.2d at 688, 2 USPQ at 1278 (Fed. Cir. 1987)

[31] See Final Office Action, p. 3, last paragraph.

facie obviousness against claim 20, claim 20 stands patentable over the references.

Conclusion

Applicant respectfully submits that because the prior art references relied upon in the Final Office Action fail to support a case of prima facie obviousness against claims 1 and 20, claims 1 and 20 stand patentable over the references. Claims 2-19, 21 and 22 also stand patentable because claims 2-19 depend properly from claim 1, and claims 21 and 22 properly depend from claim 20. Applicants respectfully request the Board to reverse the final rejection and allow claims 1-22 on appeal.

Respectfully submitted,

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APPENDIX

The claims on appeal read as follows:

1. (original) A semiconductor device including a contact pad and circuit metallization on the surface of an integrated circuit chip, comprising:

a stack of protection layers over the surface of said chip, said stack comprising a first inorganic layer on said surface, a polymer layer on said first inorganic layer, and a second inorganic layer on said polymer layer;

a window in said stack of layers exposing said metallization on said integrated circuit chip;

a patterned seed metal layer on said metallization in said window and on said second inorganic layer around said window; and

buffer metal layer positioned on said seed metal layer.

2. (original) The device according to Claim 1 wherein said interconnecting metallization comprises copper.

3. (original) The device according to Claim 1 wherein said first inorganic layer comprises silicon nitride.

4. (original) The device according to Claim 1 wherein said first inorganic layer is selected from a group consisting of silicon nitride, silicon oxynitride, silicon carbide, polyimide, and stacked layer of said materials.

5. (original) The device according to Claim 1 wherein said first inorganic layer has a thickness in the range from about 0.5 to 2 μm.

6. (original) The device according to Claim 1 wherein said polymer layer comprises benzocyclobutene or polybenzoxazole.

7. (original) The device according to Claim 1 wherein said polymer layer is selected from a group consisting of polyimides, polyamic acids, polybenzoxazoles, benzocyclobutenes, polybenzocyclobutenes, and polysiloxanes.

8. (original) The device according to Claim 1 wherein said polymer layer has a thickness of the range from about 3 to 10 μm.

9. (original) The device according to Claim 1 wherein said second inorganic layer comprises silicon dioxide.

10. (original) The device according to Claim 1 wherein said second inorganic layer is a dielectric selected from a group consisting of silicon dioxide, silicon nitride, silicon oxynitride, and stacked layers thereof.

11. (original) The device according to Claim 1 wherein said second inorganic layer has a thickness from about 0.5 to 2 μm.

12. (original) The device according to Claim 1 wherein said seed metal comprises copper.

13. (original) The device according to Claim 1 wherein said seed metal overlaps said second inorganic layer by an amount between about 5 and 15 μm.

14. (original) The device according to Claim 1 wherein said buffer metal comprises a single metal layer.

15. (original) The device according to Claim 14 wherein said single metal layer comprises copper or a copper alloy.

16. (original) The device according to Claim 1 wherein said buffer metal comprises a stack of metal layers.

17. (original) The device according t Claim 16 wherein said stack of metal layers comprises copper in contact with said seed metal, nickel on top of said copper, and palladium as outermost metal.

18. (original) The device according to Claim 1 further comprising a metal reflow element attached to said buffer metal.

19. (original) The device according to Claim 1 further comprising a bond wire attached to said buffer metal.

20. (original) A semiconductor device including a contact pad and circuit metallization on the surface of an integrated circuit chip, comprising:

a stack of protection layers over the surface of said chip, said stack comprising a first inorganic layer on said surface, a polymer layer on said first inorganic layer, and a second inorganic layer on said polymer layer;

a window in said stack of layers exposing said metallization on said integrated circuit chip;

a seed metal layer on said metallization in said window and on said second inorganic layer, said seed metal layer patterned to form an extended trace remote from said window; and

a patterned buffer metal layer positioned on a selected location of said seed metal layer.

21. (original) The device according to Claim 20 further comprising a metal reflow element attached to said buffer metal.

22. (original) The device according to Claim 20 further comprising a bond wire attached to said buffer metal.

23-28. (canceled)